CLAIMS

What is claimed is:

1. A method for processing television signals, the method comprising:

receiving an inband signal by a single chip integrated DTV receiver;

demodulating said received inband signal within said single chip DTV receiver;

receiving an out-of-band signal corresponding to said received inband signal by said single chip integrated DTV receiver; and

processing said received out-of-band signal within said single chip integrated DTV receiver.

2. The method according to claim 1, wherein said received inband signal is one of a VSB signal, a NTSC signal, and a QAM signal.

3. The method according to claim 1, further comprising:

if said received inband signal is a VSB signal, error correcting said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ATSC compliant signal; and

if said received inband signal is a QAM signal, error correcting said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ITU-T J.83 compliant signal.

4. The method according to claim 3, wherein said ITU-T J.83 compliant signal is compliant with at least one of Annex A, Annex B and Annex C of ITU-T J.83.

05. The method according to claim 3, further comprising:

if said received inband signal is a VSB signal, equalizing said error corrected ATSC signal within said single chip integrated DTV receiver; and

if said received inband signal is a QAM signal, equalizing said error corrected ITU-T J.83 compliant signal within said single chip integrated DTV receiver.

6. The method according to claim 1, further comprising generating from within said single chip integrated DTV receiver, an output MPEG transport stream from said demodulated received inband signal.

7. The method according to clam 6, wherein said output MPEG transport stream is a serial MPEG transport stream or a parallel MPEG transport stream.

8. The method according to claim 1, further comprising if said received inband signal is an NTSC signal, decoding said demodulated received inband signal within said single chip integrated DTV receiver.

9. The method according to claim 8, further comprising generating from within said single chip integrated DTV receiver, at least one of an I^2S audio output, a stereo audio output, a monaural audio output, and a multiplexed baseband audio output from said decoded demodulated received inband signal.

10. The method according to claim 1, further comprising if said received signal is an NTSC signal, generating a composite NTSC signal from said demodulated received signal within said single chip integrated DTV receiver.

11. The method according to claim 1, further comprising demodulating said received out-of-band signal within said single chip integrated DTV receiver.

12. The method according to claim 11, further comprising demodulating said received out-of-band signal within said single chip integrated DTV receiver utilizing a QPSK demodulator.

13. The method according to claim 11, further comprising error correcting said demodulated received out-of-band signal within said single chip integrated DTV receiver.

14. The method according to claim 1, further comprising generating an output out-of-band transport stream from said processed received out-of-band signal from within said single chip integrated DTV receiver.

15. The method according to claim 14, wherein said out-of-band transport stream comprises CableCard encryption and security data.

16. The method according to claim 1, further comprising controlling said demodulating of said received inband signal via an on-chip processor integrated within said single chip integrated DTV receiver.

17. A machine-readable storage having stored thereon, a computer program having at least one code section for processing television signals, the at least one code section being executable by a machine for causing the machine to perform steps comprising:

receiving an inband signal by a single chip integrated DTV receiver;

demodulating said received inband signal within said single chip DTV receiver;

receiving an out-of-band signal corresponding to said received signal by said single chip integrated DTV receiver; and

processing said received out-of-band signal within said single chip integrated DTV receiver.

18. The machine-readable storage according to claim 17, wherein said received signal is one of a VSB signal, a NTSC signal, and a QAM signal.

19. The machine-readable storage according to claim 17, further comprising:

code for error correcting said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ATSC compliant signal, if said received inband signal is a VSB signal; and

code for error correcting said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ITU-T J.83 compliant signal, if said received inband signal is a QAM signal.

20. The machine-readable storage according to claim 19, wherein said ITU-T J.83 compliant signal is compliant with at least one of Annex A, Annex B and Annex C of ITU-T J.83.

21. The machine-readable storage according to claim 19, further comprising:

code for equalizing said error corrected ATSC signal within said single chip integrated DTV receiver, if said received inband signal is a VSB signal; and

code for equalizing said error corrected ITU-T J.83 compliant signal within said single chip integrated DTV receiver, if said received inband signal is a QAM signal.

22. The machine-readable storage according to claim 17, further comprising code for generating from within said single chip integrated DTV receiver, an output MPEG transport stream from said demodulated received inband signal.

23. The machine-readable storage according to clam 22, wherein said output MPEG transport stream is a serial MPEG transport stream or a parallel MPEG transport stream.

24. The machine-readable storage according to claim 17, further comprising code for decoding said demodulated received signal within said single chip integrated DTV receiver, if said received inband signal is an NTSC signal.

25. The machine-readable storage according to claim 24, further comprising code for generating from within said single chip integrated DTV receiver, at least one of an I^2S audio output, a stereo audio output, a monaural audio output, and a multiplexed baseband audio output from said decoded demodulated received inband signal.

26. The machine-readable storage according to claim 17, further comprising code for generating a composite NTSC signal from said demodulated received signal within said single chip integrated DTV receiver, if said received inband signal is an NTSC signal.

27. The machine-readable storage according to claim 17, further comprising code for demodulating said received out-of-band signal within said single chip integrated DTV receiver.

28. The machine-readable storage according to claim 27, further comprising code for demodulating said received out-of-band signal within said single chip integrated DTV receiver utilizing a QPSK demodulator.

29. The machine-readable storage according to claim 27, further comprising code for error correcting said demodulated received out-of-band signal within said single chip integrated DTV receiver.

30. The machine-readable storage according to claim 17, further comprising code for generating an output out-of-band transport stream from said processed received out-of-band signal from within said single chip integrated DTV receiver.

31. The machine-readable storage according to claim 30, wherein said out-of-band transport stream comprises CableCard encryption and security data.

32. The machine-readable storage according to claim 17, further comprising code for controlling said demodulating of said received inband signal via an on-chip processor integrated within said single chip integrated DTV receiver

33. A system for processing television signals, the system comprising:

an inband analog front end integrated in a single chip integrated DTV receiver that receives an inband signal;

a demodulator within said single chip DTV receiver that demodulates said received inband signal;

an out-of-band analog front end integrated in said single chip integrated DTV receiver that receives an out-of-band signal corresponding to said received signal by; and

an out-of band receiver integrated within said single chip integrated DTV receiver that processes said received out-of-band signal.

34. The system according to claim 33, wherein said received inband signal is one of a VSB signal, a NTSC signal, and a QAM signal.

35. The system according to claim 33, further comprising:

an ATSC FEC that error corrects said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ATSC compliant signal, if said received inband signal is a VSB signal; and

and ITU-T J.83 compliant FEC that error corrects said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ITU-T J.83 compliant signal if said received signal is a QAM signal.

36. The system according to claim 35, wherein said ITU-T J.83 compliant signal is compliant with at least one of Annex A, Annex B and Annex C of ITU-T J.83.

37. The system according to claim 35, further comprising:

at least one equalizer that equalizes said error corrected ATSC signal within said single chip integrated DTV receiver, if said received inband signal is a VSB signal; and

said at least one equalizer equalizes said error corrected ITU-T J.83 compliant signal within said single chip integrated DTV receiver, if said received inband signal is a QAM signal.

38. The system according to claim 33, further comprising and inband output interface that generates from within said single chip integrated DTV receiver, an output MPEG transport stream from said demodulated received inband signal.

39. The system according to clam 38, wherein said output MPEG transport stream is a serial MPEG transport stream or a parallel MPEG transport stream.

40. The system according to claim 33, further comprising a BTSC decoder that decodes said demodulated received inband signal within said single chip integrated DTV receiver if said received inband signal is an NTSC signal.

41. The system according to claim 40, further comprising at least one of said BTSC decoder and an audio DAC that generates from within said single chip integrated DTV receiver, at least one of an I^2S audio output, a stereo audio output, a monaural audio output, and a multiplexed baseband audio output from said decoded demodulated received inband signal.

42. The system according to claim 33, further comprising a DAC that generates a composite NTSC signal from said demodulated received inband signal within said single chip integrated DTV receiver if said received inband signal is an NTSC signal.

43. The system according to claim 33, further comprising a demodulator that demodulates said received out-of-band signal within said single chip integrated DTV receiver.

44. The system according to claim 33, further comprising a QPSK demodulator that demodulates said received out-of-band signal within said single chip integrated DTV receiver utilizing.

45. The system according to claim 43, further comprising at least one of a DVS-167 compliant FEC and a DVS-178 compliant FEC that error corrects said demodulated received out-of-band signal within said single chip integrated DTV receiver.

46. The system according to claim 33, further comprising an out-of-band output interface that generates an output out-of-band transport stream from said processed received out-of-band signal from within said single chip integrated DTV receiver.

47. The system according to claim 46, wherein said out-of-band transport stream comprises CableCard encryption and security data.

48. The system according to claim 33, further comprising an on-chip processor that controls said demodulating of said received inband signal within said single chip integrated DTV receiver.

49. The system according to claim 33, further comprising further comprising a third overtone crystal which generates a 54 MHz clock signal which is coupled to said inband analog front end.